

CMOS 80 MHz, Triple 8-Bit Video DAC

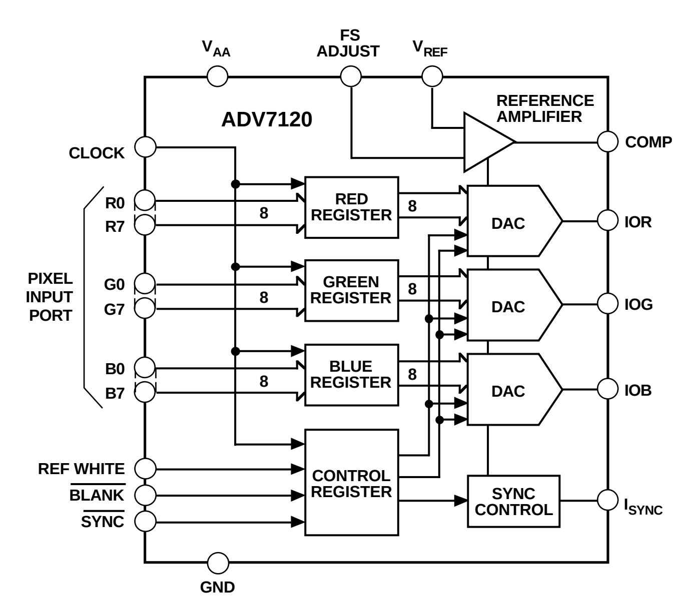
ADV7120

FEATURES
80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP or 44-Pin PLCC and 48-Lead TQFP

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing
Direct Digital Synthesis (DDS) and I/Q Modulation

SPEED GRADES*
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7120 (ADV®) is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It is also ideal for any high speed communications type applications requiring low cost, high speed DACs. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV7120 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include composite sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV7120 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV7120 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC. The ADV7120 is also available in a very small 48-lead Thin Quad Flatpack (TQFP).

ADV is a registered trademark of Analog Devices, Inc.
***Speed grades up to 140 MHz are also available upon special request. Please contact Analog Devices or its representatives for further details.**

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

REV. B

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ADV7120–SPECIFICATIONS

(V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	All Versions	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution (Each DAC)	8	Bits	
Accuracy (Each DAC)			
Integral Nonlinearity, INL	±1	LSB max	
Differential Nonlinearity, DNL	±0.5	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale max	Max Gray Scale Current: IOG = (V_{REF}* 12,082/R_{SET}) mA
			IOR, IOB = (V_{REF}* 8,627/R_{SET}) mA
Coding	Binary		
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Current, I_{IN}	±1	µA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}[2]	10	pF max	
ANALOG OUTPUTS			
Gray Scale Current Range	15	mA min	
	22	mA max	
Output Current			
White Level Relative to Blank	17.69	mA min	Typically 19.05 mA
	20.40	mA max	
White Level Relative to Black	16.74	mA min	Typically 17.62 mA
	18.50	mA max	
Black Level Relative to Blank	0.95	mA min	Typically 1.44 mA
	1.90	mA max	
Blank Level on IOR, IOB	0	µA min	Typically 5 µA
	50	µA max	
Blank Level on IOG	6.29	mA min	Typically 7.62 mA
	9.5	mA max	
Sync Level on IOG	0	µA min	Typically 5 µA
	50	µA max	
LSB Size	69.1	µA typ	
DAC to DAC Matching	5	% max	Typically 2%
Output Compliance, V_{OC}	–1	V min	
	+1.4	V max	
Output Impedance, R_{OUT}[2]	100	kΩ typ	
Output Capacitance, C_{OUT}[2]	30	pF max	I_{OUT} = 0 mA
VOLTAGE REFERENCE			
Voltage Reference Range, V_{REF}	1.14/1.26	V min/V max	V_{REF} = 1.235 V for Specified Performance
Input Current, I_{VREF}	–5	mA typ	
POWER REQUIREMENTS			
V_{AA}	5	V nom	
I_{AA}	125	mA max	Typically 80 mA: 80 MHz Parts
	100	mA max	Typically 70 mA: 50 MHz & 35 MHz Parts
Power Supply Rejection Ratio	0.5	%/% max	Typically 0.12%/%: f = 1 kHz, COMP = 0.1 µF
Power Dissipation	625	mW max	Typically 400 mW: 80 MHz Parts
	500	mW max	Typically 350 mW: 50 MHz & 30 MHz Parts
DYNAMIC PERFORMANCE			
Glitch Impulse[2, 3]	50	pV secs typ	
DAC Noise[2, 3, 4]	200	pV secs typ	
Analog Output Skew	2	ns max	Typically 1 ns

NOTES

[1]Temperature range (T_{MIN} to T_{MAX}); 0°C to +70°C.

[2]Sample tested at +25°C to ensure compliance.

[3]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

[4]This includes effects due to clock and data feedthrough as well as RGB analog crosstalk.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{AA} = +5 V ± 5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ω. I_{SYNC} connected to IOG. All Specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	80 MHz Version	50 MHz Version	30 MHz Version	Units	Conditions/Comments
f_{MAX}	80	50	30	MHz max	Clock Rate
t_1	3	6	8	ns min	Data & Control Setup Time
t_2	2	2	2	ns min	Data & Control Hold Time
t_3	12.5	20	33.3	ns min	Clock Cycle Time
t_4	4	7	9	ns min	Clock Pulse Width High Time
t_5	4	7	9	ns min	Clock Pulse Width Low Time
t_6	30	30	30	ns max	Analog Output Delay
	20	20	20	ns typ	
t_7	3	3	3	ns max	Analog Output Rise/Fall Time
t_8[3]	12	15	15	ns typ	Analog Output Transition Time

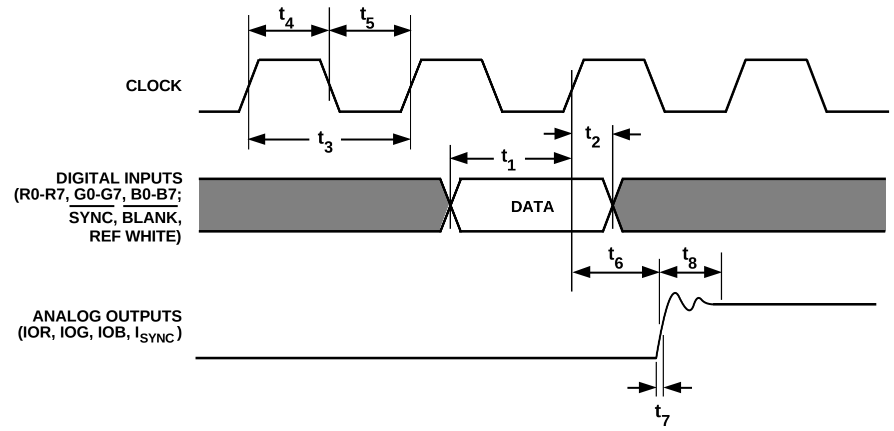
NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.

[2]Temperature range (T_{MIN} to T_{MAX}): 0°C to +70°C

[3]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.
3. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL TRANSITION.

Figure 1. Video Input/Output Timing

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . +7 V
Voltage on Any Digital Pin . . . . . GND –0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . +150°C
Soldering Temperature (10 secs) . . . . 300°C
Vapor Phase Soldering (1 minute) . . . . 220°C
IOR, IOB, IOG, I_{SYNC} to GND[2] . . . . 0 V to V_{AA}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model	Speed	Temperature Range[1]	Package Option[2]
ADV7120KN80	80 MHz	0°C to +70°C	N-40A
ADV7120KN50	50 MHz	0°C to +70°C	N-40A
ADV7120KN30	30 MHz	0°C to +70°C	N-40A
ADV7120KP80	80 MHz	0°C to +70°C	P-44A
ADV7120KP50	50 MHz	0°C to +70°C	P-44A
ADV7120KP30	30 MHz	0°C to +70°C	P-44A
ADV7120KST50	50 MHz	0°C to +70°C	ST-48
ADV7120KST30	30 MHz	0°C to +70°C	ST-48

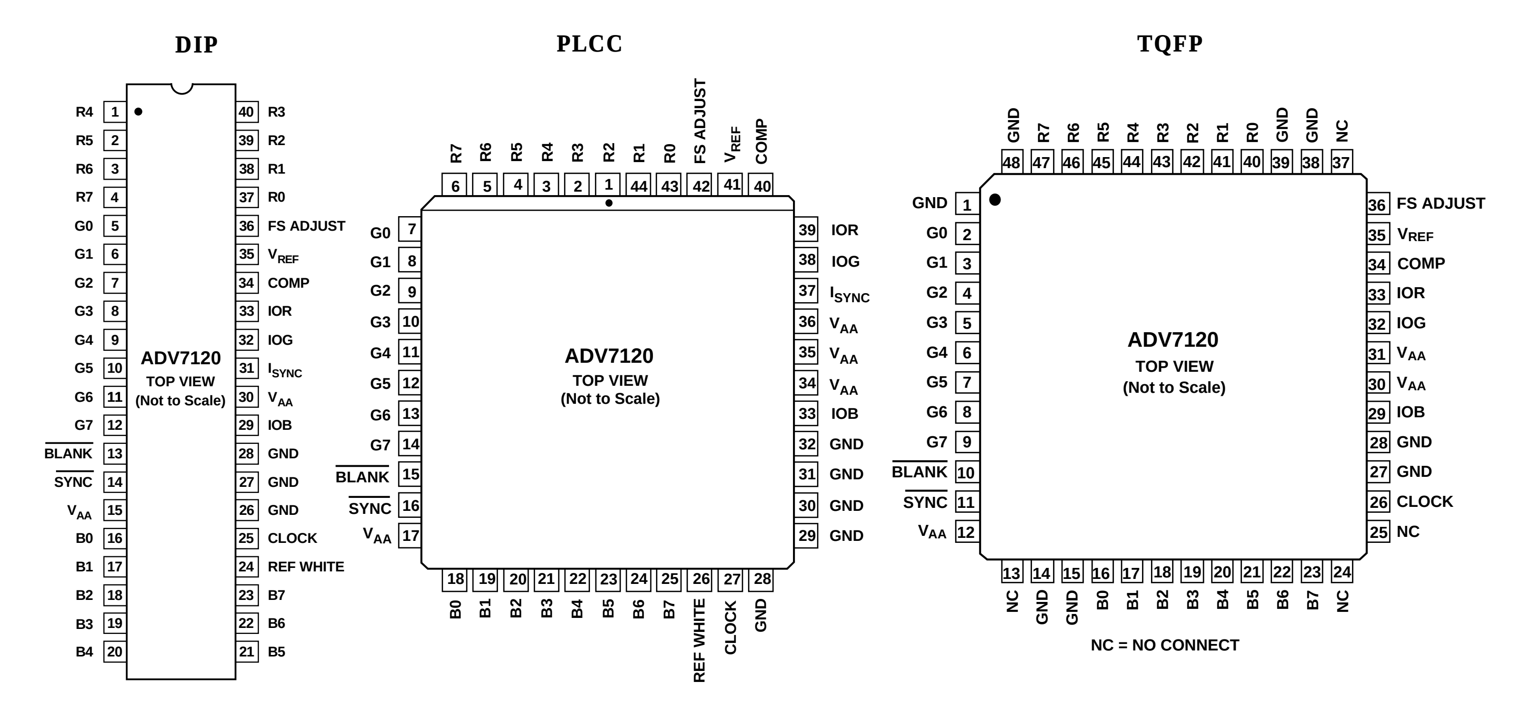
NOTES
[1]Industrial temperature range (–40°C to +85°C) version available to special request. Please consult your local Analog Device representative.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7120 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS



NOTE
For the ADV7120 in TQFP package: The REF WHITE pin is not available.
The I_{SYNC} pin is not available and is internally connected to the IOG pin.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{BLANK}$	Composite blank control input (TTL compatible). A logic zero on this control input drives the analog outputs, IOR, IOB and IOG, to the blanking level. The $\overline{BLANK}$ signal is latched on the rising edge of CLOCK. While $\overline{BLANK}$ is a logical zero, the R0–R7, G0–G7, R0–R7 and REF WHITE pixel and control inputs are ignored.
$\overline{SYNC}$	Composite sync control input (TTL compatible). A logical zero on the $\overline{SYNC}$ input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{SYNC}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{SYNC}$ is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, $\overline{SYNC}$, $\overline{BLANK}$ and REF WHITE pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the pixel input data (R0–R7, G0–G7 and B0–B7). REF WHITE is latched on the rising edge of clock.
R0–R7, G0–G7, B0–B7	Red, green and blue pixel data inputs (TTL compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0 and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular PCB power or ground plane.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
I_{SYNC}	Sync current output. This high impedance current source can be directly connected to the IOG output. This allows sync information to be encoded onto the green channel. I_{SYNC} does not output any current while $\overline{SYNC}$ is at logical zero. The amount of current output at I_{SYNC} while $\overline{SYNC}$ is at logical one is given by: $I_{SYNC}\ (mA) = 3{,}455 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$ If sync information is not required on the green channel, I_{SYNC} should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: $R_{SET}\ (\Omega) = 12{,}082 \times V_{REF}\ (V) / IOG\ (mA)$ The relationship between R_{SET} and the full-scale output current on IOR and IOB is given by: $IOR, IOB\ (mA) = 8{,}628 \times V_{REF}\ (V) / R_{SET}\ (\Omega)$
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.2 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 µF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7120 must be connected.
GND	Ground. All GND pins must be connected.

TERMINOLOGY

Blanking Level

The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)

This usually refers to the technique of combining the three primary colors of red, green and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)

The position of the composite video signal which synchronizes the scanning process.

Gray Scale

The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels while a 6-bit DAC contains 64.

Raster Scan

The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level

The maximum negative polarity amplitude of the video signal.

Reference White Level

The maximum positive polarity amplitude of the video signal.

Sync Level

The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal

That portion of the composite video signal which varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion which may be visually observed.

CIRCUIT DESCRIPTION AND OPERATION

The ADV7120 contains three 8-bit D/A converters, with three input channels each containing an 8-bit register. Also integrated on board the part is a reference amplifier and CRT control functions $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE.

Digital Inputs

24-bits of pixel data (color information) R0–R7, G0–G7 and B0–B7 are latched into the device on the rising edge of each clock cycle. This data is presented to the three 8-bit DACs and is then converted to three analog (RGB) output waveforms. (See Figure 2.)

Three other digital control signals are latched to the analog video outputs in a similar fashion. $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs. Figure 3 shows the analog output, RGB video waveform of the ADV7120. The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated.

The REF WHITE control input drives the RGB video outputs to the white level. This function could be used to overlay a cursor or crosshair onto the RGB video output.

Table I details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE.

All these digital inputs are specified to accept TTL logic levels.

Clock Input

The CLOCK input of the ADV7120 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and hence the required CLOCK frequency, will be determined by the on-screen resolution, according to the following equation:

Dot Rate = (Horiz: Res) × (Vert Res) × (Refresh Rate)/ (Retrace Factor)

Horiz Res	=	Number of pixels/line
Vert Res	=	Number of lines/frame
Refresh Rate	=	Horizontal scan rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system or 30 Hz for an interlaced system.
Retrace Factor	=	Total blank time factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (e.g., 0.8).

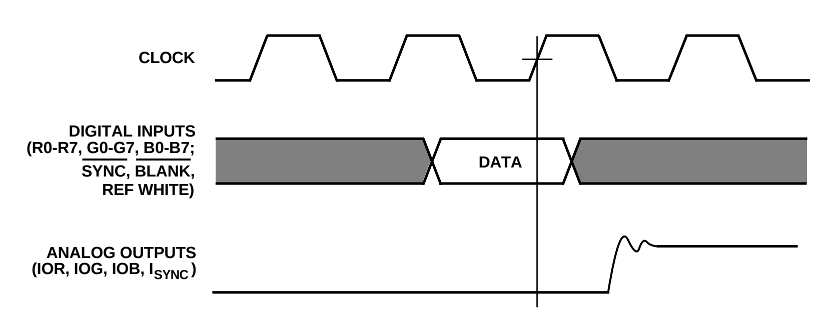


Figure 2. Video Data Input/Output

If we, therefore, have a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate and a retrace factor of 0.8, then:

Dot Rate = 1024 × 1024 × 60/0.8
= 78.6 MHz

The required CLOCK frequency is thus 78.6 MHz.

All video data and control inputs are latched into the ADV7120 on the rising edge of CLOCK, as previously described in the "Digital Inputs" section. It is recommended that the CLOCK input to the ADV7120 be driven by a TTL buffer (e.g., 74F244).

RED, BLUE		GREEN		
mA	V	mA	V	
19.05	0.714	26.67	1.000	WHITE LEVEL
1.44	0.054	9.05	0.340	BLACK LEVEL
0	0	7.62	0.286	BLANK LEVEL
		0	0	SYNC LEVEL

NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 560Ω, I_{SYNC} CONNECTED TO IOG.
3. RS-343A LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure 3. RGB Video Output Waveform

Table I. Video Output Truth Table

Description	IOG (mA)[1]	IOR, IOB (mA)	REF WHITE	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	1	xxH
WHITE LEVEL	26.67	19.05	0	1	1	FFH
VIDEO	video + 9.05	video + 1.44	0	1	1	data
VIDEO to BLANK	video + 1.44	video + 1.44	0	0	1	data
BLACK LEVEL	9.05	1.44	0	1	1	00H
BLACK to BLANK	1.44	1.44	0	0	1	00H
BLANK LEVEL	7.62	0	0	1	0	xxH
SYNC LEVEL	0	0	0	0	0	xxH

NOTE
Typical with full-scale IOG = 26.67 mA.
V_{REF} = 1.235 V, R_{SET} = 560 Ω, I_{SYNC} connected to IOG.

Video Synchronization and Control

The ADV7120 has a single composite video sync ($\overline{SYNC}$) input control. Many graphics processors and CRT controllers have the ability of generating horizontal sync (HSYNC), vertical sync (VSYNC) and composite $\overline{SYNC}$.

In a graphics system which does not automatically generate a composite $\overline{SYNC}$ signal, the inclusion of some additional logic circuitry will enable the generation of a composite $\overline{SYNC}$ signal.

The I_{SYNC} current output is typically connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the ADV7120's analog outputs, the $\overline{SYNC}$ input should be tied to logic low and the I_{SYNC} should be connected to analog ground.

Reference Input

An external 1.23 V voltage reference is required to drive the ADV7120. The AD589 from Analog Devices is an ideal choice of reference. It is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23 V output voltage for input currents between 50 μA and 5 mA. Figure 4 shows a typical reference circuit connection diagram. The voltage reference gets its current drive from the ADV7120's V_{AA} through an on-board 1 kΩ resistor to the V_{REF} pin. A 0.1 μF ceramic capacitor is required between the COMP pin and V_{AA}. This is necessary so as to provide compensation for the internal reference amplifier.

A resistance R_{SET} connected between FS ADJUST and GND determines the amplitude of the output video level according to the following equations:

$$IOG\ (mA) = 12{,}082 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad (1)$$

$$IOR,\ IOB\ (mA) = 8{,}628 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad (2)$$

If $\overline{SYNC}$ is not being encoded onto the green channel, then Equation 1 will be similar to Equation 2.

Using a variable value of R_{SET}, as shown in Figure 4, allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels as quoted in the specification page. These values also correspond to the RS-343A video waveform values as shown in Figure 3.

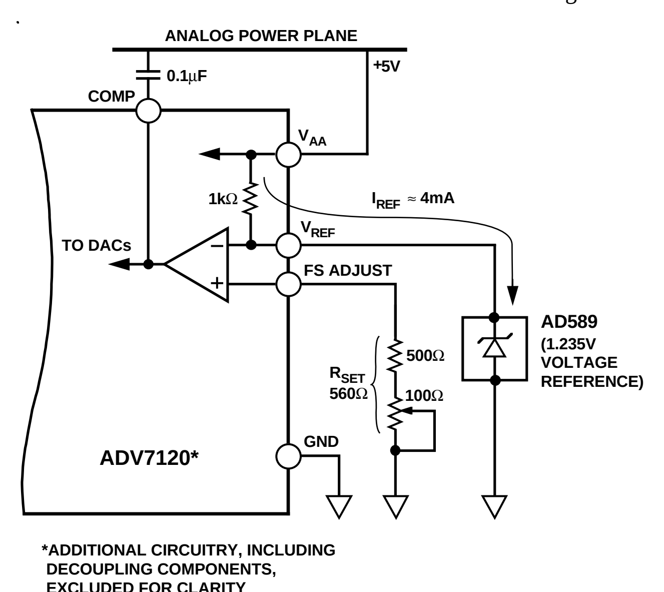


Figure 4. Reference Circuit

D/A Converters

The ADV7120 contains three matched 8-bit D/A converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = "1") or GND (bit = "0") by a sophisticated decoding scheme. As all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The onboard operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Analog Outputs

The ADV7120 has three analog outputs, corresponding to the red, green and blue video signals. A fourth analog output (I_{SYNC}) can be used if it is required to encode video synchronization information onto the green signal. In this case, I_{SYNC} is connected to IOG . (See "Video Synchronization and Control" section.)

The red, green and blue analog outputs of the ADV7102 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 5a shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75 Ω load. This arrangement will develop RS-343A video output voltage levels across a 75 Ω monitor.

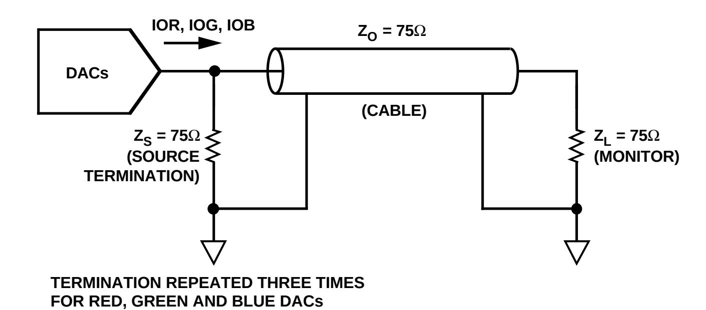


Figure 5a. Analog Output Termination for RS-343A

One suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 5b. The output current levels of the DACs remain unchanged but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

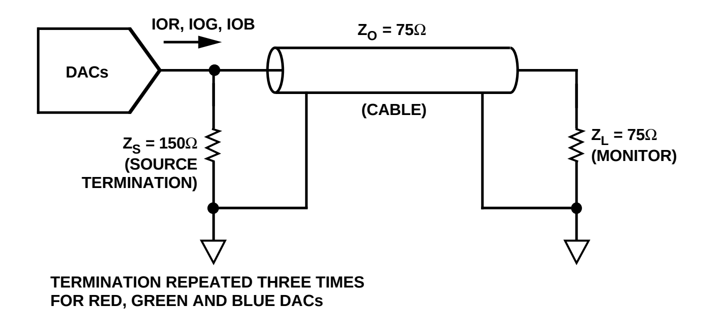


Figure 5b. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in an application note entitled "Video Formats & Required Load Terminations" available from Analog Devices, publication number E1228-15-1/89.

Figure 3 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75 Ω load of Figure 5a. As well as the gray scale levels, black level to white level, the diagram also shows the contributions of $\overline{SYNC}$ and $\overline{BLANK}$. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table I details how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

Gray Scale Operation

The ADV7120 can be used for stand-alone, gray scale (monochrome) or composite video applications (i.e., only one channel used for video information). Any one of the three channels, red, green or blue, can be used to input the digital video data. The two unused video data channels should be tied to logical zero.

The unused analog outputs should be terminated with the same load as that for the used channel. In other words, if the red channel is used and IOR is terminated with a doubly terminated 75 Ω load (37.5 Ω), IOB and IOG should be terminated with 37.5 Ω resistors. (See Figure 6.)

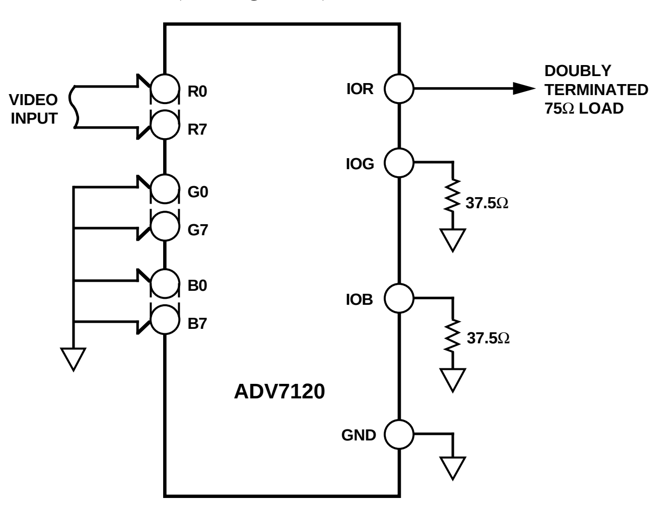


Figure 6. Input and Output Connections for Stand-Alone Gray Scale or Composite Video

Video Output Buffers

The ADV7120 is specified to drive transmission line loads, which is what most monitors are rated as. The analog output configurations to drive such loads are described in the Analog Interface section and illustrated in Figure 5. However, in some applications it may be required to drive long "transmission line" cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers will compensate for some cable distortion. Buffers with large full power bandwidths and gains between 2 and 4 will be required.

These buffers will also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD84X series of monolithic op amps. In very high frequency applications (80 MHz), the AD9617 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit will result in any desired video level.

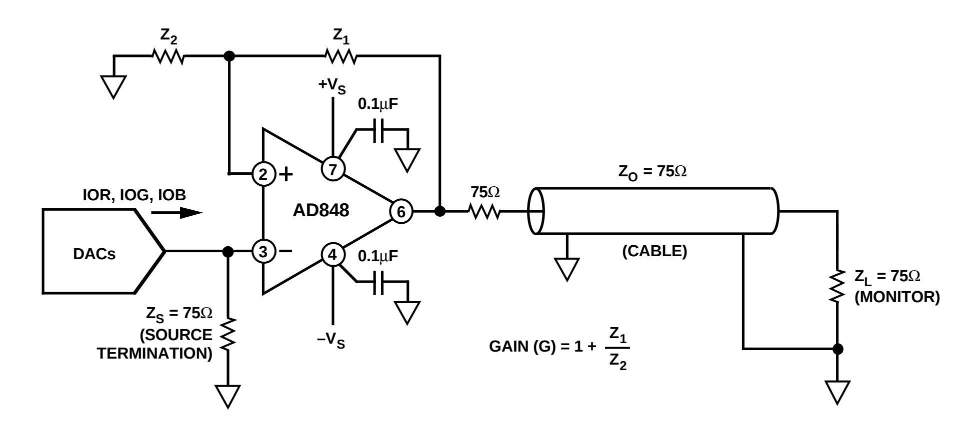


Figure 7. AD848 As an Output Buffer

PC BOARD LAYOUT CONSIDERATIONS

The ADV7120 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7120, it is imperative that great care be given to the PC board layout. Figure 8 shows a recommended connection diagram for the ADV7120.

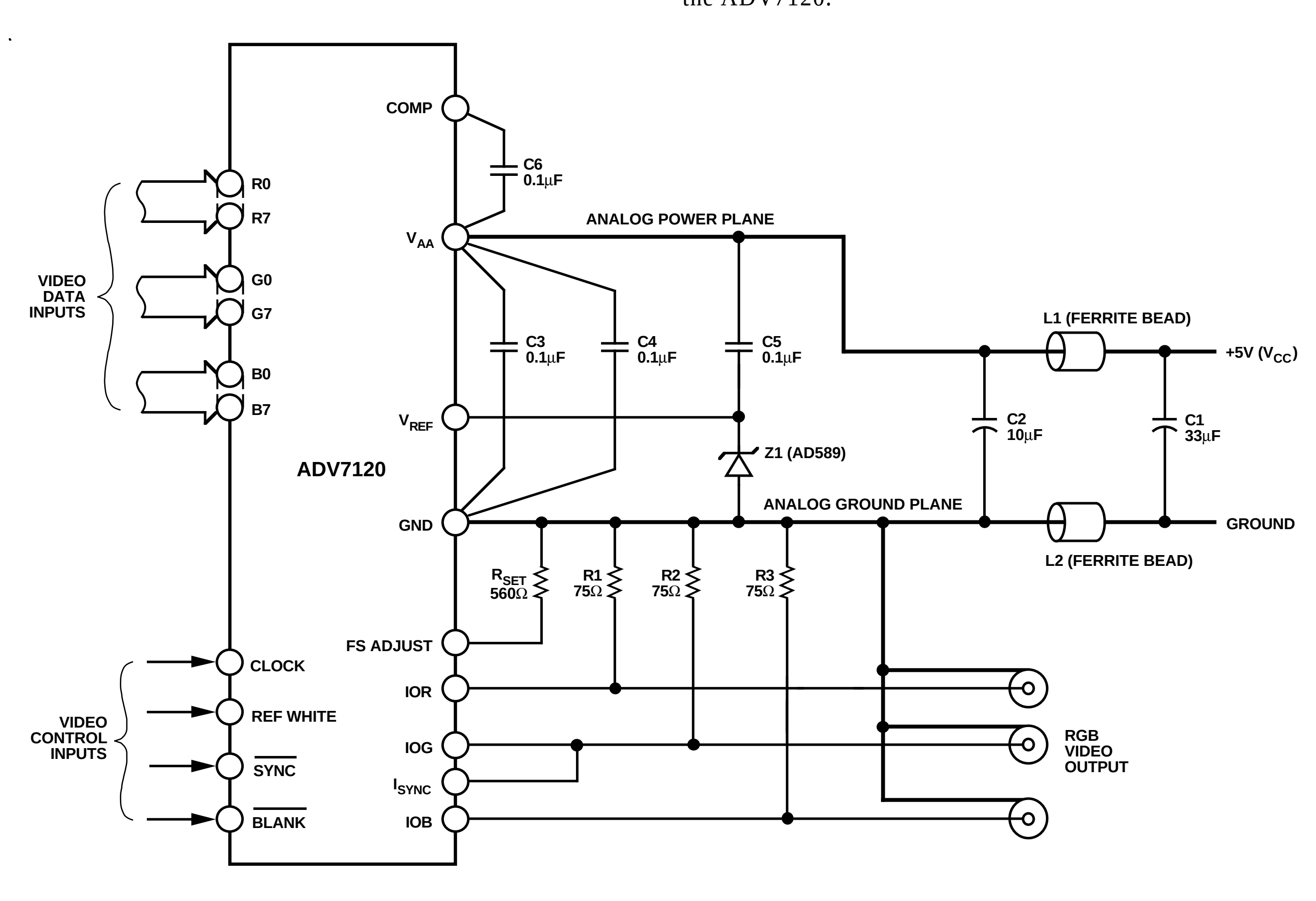
The layout should be optimized for lowest noise on the ADV7120 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ADV7120 and associated analog circuitry, should have a separate ground plane referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located as close as possible (within 3 inches) to the ADV7120.

The analog ground plane should encompass all ADV7120 ground pins, voltage reference circuitry, power supply bypass circuitry, the analog output traces and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the ADV7120.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1	33µF TANTALUM CAPACITOR	
C2	10µF TANTALUM CAPACITOR	
C3, C4, C5, C6	0.1µF CERAMIC CAPACITOR	
L1, L2	FERRITE BEAD	FAIR-RITE 274300111 OR MURATA BL01/02/03
R1, R2, R3	75Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R_{SET}	560Ω 1% METAL FILM RESISTOR	DALE CMF-55C
Z1	1.235V VOLTAGE REFERENCE	ANALOG DEVICES AD589JH

Figure 8. ADV7120 Typical Connection Diagram and Component List

Power Planes

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the ADV7120 (V_{AA}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead, as illustrated in Figure 8. This bead should be located within three inches of the ADV7120.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7120 power pins, voltage reference circuitry and any output amplifiers.

The PCB power and ground planes should not overlay portions of the analog power plane. Keeping the PCB power and ground planes from overlaying the analog power plane will contribute to a reduction in plane-to-plane noise coupling.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of multiple decoupling capacitors. (See Figure 8.)

Optimum performance is achieved by the use of 0.1 μF ceramic capacitors. Each of the two groups of V_{AA} should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

It is important to note that while the ADV7120 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) will provide EMI suppression between the switching power supply and the main PCB. Alternatively, consideration could be given to using a three terminal voltage regulator.

Digital Signal Interconnect

The digital signal lines to the ADV7120 should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7120 should be avoided so as to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7120 should be located as close as possible to the output connectors thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, thereby maximizing the high frequency power supply rejection.

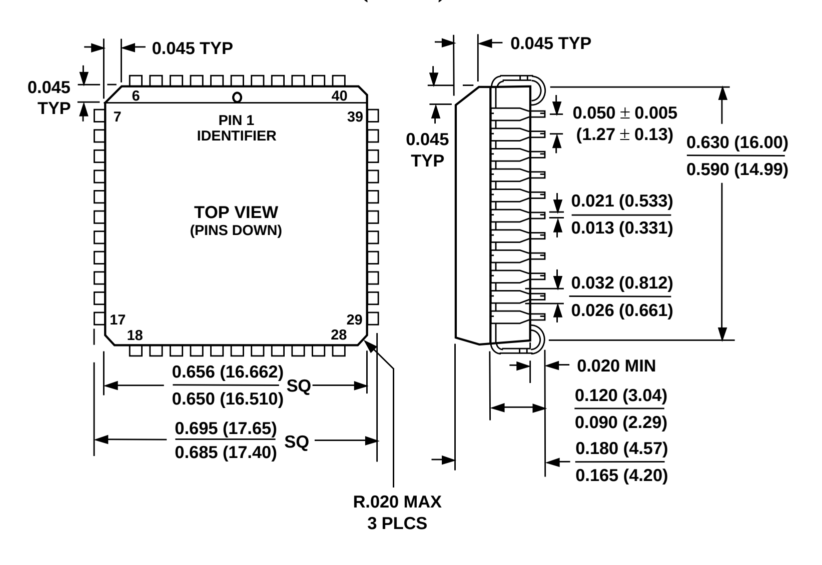
For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7120 so as to minimize reflections.

Additional information on PCB design is available in an application note entitled “Design and Layout of a Video Graphics System for Reduced EMI.” This application note is available from Analog Devices, publication number E1309-15-10/89.

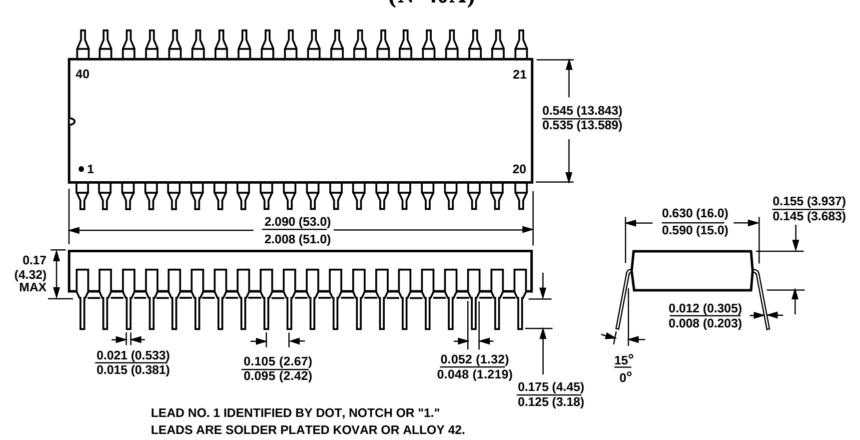
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Terminal Plastic Leaded Chip Carrier (P-44A)

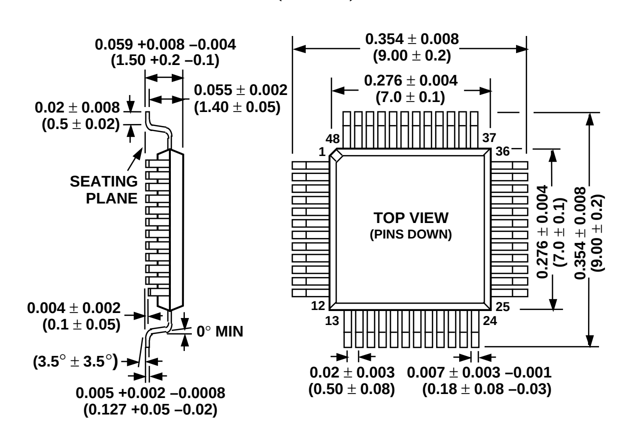


40-Pin Plastic DIP (N-40A)



LEAD NO. 1 IDENTIFIED BY DOT, NOTCH OR "1."
LEADS ARE SOLDER PLATED KOVAR OR ALLOY 42.

48-Lead TQFP (ST-48)



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